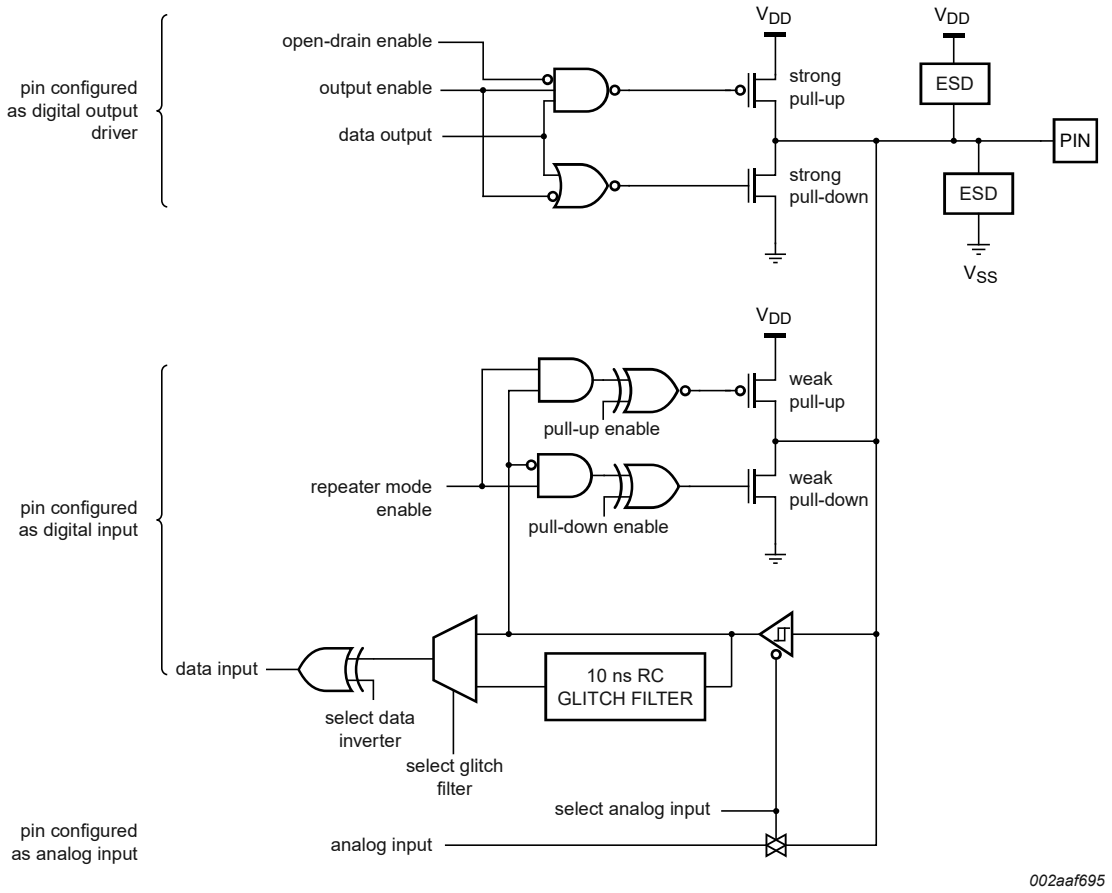

The 10 ns glitch filter is available on selected pins only.

Fig 13. Standard I/O pin configuration

7.3.1 Pin function

The FUNC bits in the IOCON registers can be set to GPIO (FUNC = 000) or to a peripheral function. If the pins are GPIO pins, the DIR registers determine whether the pin is configured as an input or output (see Section 9.5.3.3). For any peripheral function, the pin direction is controlled automatically depending on the pin's functionality. The DIR registers have no effect for peripheral functions.

7.3.2 Pin mode

The MODE bits in the IOCON register allow the selection of on-chip pull-up or pull-down resistors for each pin or select the repeater mode.

The possible on-chip resistor configurations are pull-up enabled, pull-down enabled, or no pull-up/pull-down. The default value is pull-up enabled.

The repeater mode enables the pull-up resistor if the pin is at a logic HIGH and enables the pull-down resistor if the pin is at a logic LOW. This causes the pin to retain its last known state if it is configured as an input and is not driven externally. The state retention is

Table 75. Register overview: I/O configuration (base address 0x4004 4000) *…continued*

Name	Access	Address offset	Description	Reset value	Reference
PIO1_22	R/W	0x0B8	I/O configuration for pin PIO1_22/$\overline{\text{RI}}$/MOSI1	0x0000 0090	Table 122
PIO1_23	R/W	0x0BC	I/O configuration for pin PIO1_23/CT16B1_MAT1/SSEL1	0x0000 0090	Table 123
PIO1_24	R/W	0x0C0	I/O configuration for pin PIO1_24/ CT32B0_MAT0	0x0000 0090	Table 124
PIO1_25	R/W	0x0C4	I/O configuration for pin PIO1_25/CT32B0_MAT1	0x0000 0090	Table 125
PIO1_26	R/W	0x0C8	I/O configuration for pin PIO1_26/CT32B0_MAT2/RXD/IOH_19	0x0000 0090	Table 126
PIO1_27	R/W	0x0CC	I/O configuration for pin PIO1_27/CT32B0_MAT3/TXD/IOH_20	0x0000 0090	Table 127
PIO1_28	R/W	0x0D0	I/O configuration for pin PIO1_28/CT32B0_CAP0/SCLK	0x0000 0090	Table 128
PIO1_29	R/W	0x0D4	I/O configuration for pin PIO1_29/SCK0/ CT32B0_CAP1	0x0000 0090	Table 129
-	R/W	0x0D8	Reserved	-	-
PIO1_31	R/W	0x0DC	I/O configuration for pin PIO1_31	0x0000 0090	Table 130

7.4.1 I/O configuration registers

7.4.1.1 RESET_PIO0_0 register

Table 76. RESET_PIO0_0 register (RESET_PIO0_0, address 0x4004 4000) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. Values 0x2 to 0x7 are reserved.	000
		0x0	$\overline{\text{RESET}}$.	
		0x1	PIO0_0.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
6	INV		Invert input	0
		0	Input not inverted (HIGH on pin reads as 1, LOW on pin reads as 0).	
		1	Input inverted (HIGH on pin reads as 0, LOW on pin reads as 1).	
9:7	-	-	Reserved.	001

Table 125. PIO1_25 register (PIO1_25, address 0x4004 40C4) bit description *...continued*

Bit	Symbol	Value	Description	Reset value
6	INV		Invert input	0
		0	Input not inverted (HIGH on pin reads as 1, LOW on pin reads as 0).	
		1	Input inverted (HIGH on pin reads as 0, LOW on pin reads as 1).	
9:7	-	-	Reserved.	001
10	OD		Open-drain mode.	0
		0	Disable.	
		1	Open-drain mode enabled. **Remark:** This is not a true open-drain mode.	
31:11	-	-	Reserved.	0

7.4.1.51 PIO1_26 register

Table 126. PIO1_26 register (PIO1_26, address 0x4004 40C8) bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. Values 0x4 to 0x7 are reserved.	000
		0x0	PIO1_26.	
		0x1	CT32B0_MAT2.	
		0x2	RXD.	
		0x3	IOH_19.	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	10
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable.	
		1	Enable.	
6	INV		Invert input	0
		0	Input not inverted (HIGH on pin reads as 1, LOW on pin reads as 0).	
		1	Input inverted (HIGH on pin reads as 0, LOW on pin reads as 1).	
9:7	-	-	Reserved.	001
10	OD		Open-drain mode.	0
		0	Disable.	
		1	Open-drain mode enabled. **Remark:** This is not a true open-drain mode.	
31:11	-	-	Reserved.	0

Table 139. Register overview: GPIO GROUP1 interrupt (base address 0x4006 0000)

Name	Access	Address offset	Description	Reset value	Reference
CTRL	R/W	0x000	GPIO grouped interrupt control register	0	Table 151
PORT_POL0	R/W	0x020	GPIO grouped interrupt port 0 polarity register	0xFFFF FFFF	Table 152
PORT_POL1	R/W	0x024	GPIO grouped interrupt port 1 polarity register	0xFFFF FFFF	Table 153
PORT_ENA0	R/W	0x040	GPIO grouped interrupt port 0 enable register	0	Table 154
PORT_ENA1	R/W	0x044	GPIO grouped interrupt port 1 enable register	0	Table 155

GPIO port addresses can be read and written as bytes, halfwords, or words.

Table 140. Register overview: GPIO port (base address 0x5000 0000)

Name	Access	Address offset	Description	Reset value	Width	Reference
B0 to B23	R/W	0x0000 to 0x0018	Byte pin registers port 0; pins PIO0_0 to PIO0_23	ext[1]	byte (8 bit)	Table 156
B32 to B63	R/W	0x0020 to 0x002F	Byte pin registers port 1	ext[1]	byte (8 bit)	Table 157
W0 to W23	R/W	0x1000 to 0x1060	Word pin registers port 0	ext[1]	word (32 bit)	Table 158
W32 to W63	R/W	0x1080 to 0x10FC	Word pin registers port 1	ext[1]	word (32 bit)	Table 159
DIR0	R/W	0x2000	Direction registers port 0	0	word (32 bit)	Table 160
DIR1	R/W	0x2004	Direction registers port 1	0	word (32 bit)	Table 161
MASK0	R/W	0x2080	Mask register port 0	0	word (32 bit)	Table 162
MASK1	R/W	0x2084	Mask register port 1	0	word (32 bit)	Table 163
PIN0	R/W	0x2100	Port pin register port 0	ext[1]	word (32 bit)	Table 164
PIN1	R/W	0x2104	Port pin register port 1	ext[1]	word (32 bit)	Table 165
MPIN0	R/W	0x2180	Masked port register port 0	ext[1]	word (32 bit)	Table 166
MPIN1	R/W	0x2184	Masked port register port 1	ext[1]	word (32 bit)	Table 167
SET0	R/W	0x2200	Write: Set register for port 0 Read: output bits for port 0	0	word (32 bit)	Table 168
SET1	R/W	0x2204	Write: Set register for port 1 Read: output bits for port 1	0	word (32 bit)	Table 169
CLR0	WO	0x2280	Clear port 0	NA	word (32 bit)	Table 170
CLR1	WO	0x2284	Clear port 1	NA	word (32 bit)	Table 171
NOT0	WO	0x2300	Toggle port 0	NA	word (32 bit)	Table 172
NOT1	WO	0x2304	Toggle port 1	NA	word (32 bit)	Table 173

[1] “ext” in this table and subsequent tables indicates that the data read after reset depends on the state of the pin, which in turn may depend on an external source.

Table 159. GPIO port 1 word pin registers (W32 to W63, addresses 0x5000 1080 to 0x5000 10FC) bit description

Bit	Symbol	Description	Reset value	Access
31:0	PWORD	Read 0: pin is LOW. Write 0: clear output bit. Read 0xFFFF FFFF: pin is HIGH. Write any value 0x0000 0001 to 0xFFFF FFFF: set output bit. **Remark:** Only 0 or 0xFFFF FFFF can be read. Writing any value other than 0 will set the output bit.	ext	R/W

9.5.3.3 GPIO port direction registers

Each GPIO port has one direction register for configuring the port pins as inputs or outputs.

Table 160. GPIO direction port 0 register (DIR0, address 0x5000 2000) bit description

Bit	Symbol	Description	Reset value	Access
31:0	DIRP0	Selects pin direction for pin P0_n (bit 0 = P0_0, bit 1 = P0_1, ..., bit 31 = P0_31). 0 = input. 1 = output.	0	R/W

Table 161. GPIO direction port 1 register (DIR1, address 0x5000 2004) bit description

Bit	Symbol	Description	Reset value	Access
31:0	DIRP1	Selects pin direction for pin P1_n (bit 0 = P1_0, bit 1 = P1_1, ..., bit 31 = P1_31). 0 = input. 1 = output.	0	R/W

9.5.3.4 GPIO port mask registers

These registers affect writing and reading the MPORT registers. Zeroes in these registers enable reading and writing; ones disable writing and result in zeros in corresponding positions when reading.

Table 162. GPIO mask port 0 register (MASK0, address 0x5000 2080) bit description

Bit	Symbol	Description	Reset value	Access
31:0	MASKP0	Controls which bits corresponding to P0_n are active in the P0MPORT register (bit 0 = P0_0, bit 1 = P0_1, ..., bit 31 = P0_31). 0 = Read MPORT: pin state; write MPORT: load output bit. 1 = Read MPORT: 0; write MPORT: output bit not affected.	0	R/W

Table 163. GPIO mask port 1 register (MASK1, address 0x5000 2084) bit description

Bit	Symbol	Description	Reset value	Access
31:0	MASKP1	Controls which bits corresponding to P1_n are active in the P1MPORT register (bit 0 = P1_0, bit 1 = P1_1, ..., bit 31 = P1_31). 0 = Read MPORT: pin state; write MPORT: load output bit. 1 = Read MPORT: 0; write MPORT: output bit not affected.	0	R/W

9.5.3.5 GPIO port pin registers

Reading these registers returns the current state of the pins read, regardless of direction, masking, or alternate functions, except that pins configured as analog I/O always read as 0s. Writing these registers loads the output bits of the pins written to, regardless of the Mask register.

Table 164. GPIO port 0 pin register (PIN0, address 0x5000 2100) bit description

Bit	Symbol	Description	Reset value	Access
31:0	PORT0	Reads pin states or loads output bits (bit 0 = P0_0, bit 1 = P0_1, ..., bit 31 = P0_31). 0 = Read: pin is low; write: clear output bit. 1 = Read: pin is high; write: set output bit.	ext	R/W

Table 165. GPIO port 1 pin register (PIN1, address 0x5000 2104) bit description

Bit	Symbol	Description	Reset value	Access
31:0	PORT1	Reads pin states or loads output bits (bit 0 = P1_0, bit 1 = P1_1, ..., bit 31 = P1_31). 0 = Read: pin is low; write: clear output bit. 1 = Read: pin is high; write: set output bit.	ext	R/W

9.5.3.6 GPIO masked port pin registers

These registers are similar to the PORT registers, except that the value read is masked by ANDing with the inverted contents of the corresponding MASK register, and writing to one of these registers only affects output register bits that are enabled by zeros in the corresponding MASK register

Table 166. GPIO masked port 0 pin register (MPIN0, address 0x5000 2180) bit description

Bit	Symbol	Description	Reset value	Access
31:0	MPORTP0	Masked port register (bit 0 = P0_0, bit 1 = P0_1, ..., bit 31 = P0_31). 0 = Read: pin is LOW and/or the corresponding bit in the MASK register is 1; write: clear output bit if the corresponding bit in the MASK register is 0. 1 = Read: pin is HIGH and the corresponding bit in the MASK register is 0; write: set output bit if the corresponding bit in the MASK register is 0.	ext	R/W